WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
a substrate;
a plurality of gate electrodes located on the substrate;
a gate dielectric located between each gate electrode and the substrate, the gate dielectrics being substantially the same thickness;
at least one of the gate electrodes made of a first material; and
at least one of the gate electrodes made of a second material which is different from the first material.

2. The semiconductor device of claim 1 wherein the substrate is silicon on insulator.

3. The semiconductor device of claim 1 wherein the first material is polysilicon.

4. The semiconductor device of claim 1 wherein the second material is selected from the group consisting of a metal, a metal alloy, a metal silicide, and a combination thereof.

5. The semiconductor device of claim 1 wherein the second material includes a plurality of materials.

6. The semiconductor device of claim 1 wherein at least one gate dielectric is an oxide.

7. The semiconductor device of claim 1 wherein at least one gate dielectric is a high K material.

8. A semiconductor device comprising:
a substrate;
a plurality of first gate electrodes located on the substrate;

a first gate dielectric located between each first gate electrode and the substrate, the first gate dielectrics being substantially the same thickness;

at least one of the first gate electrodes made of a first material;

at least one of the first gate electrodes made of a second material which is different from the first material;

at least one second gate electrode located on the substrate, the at least one second gate electrode being made of either the first material or the second material; and

a second gate dielectric located between each at least one second gate electrode and the substrate, the second gate dielectrics having a thickness different from that of the first gate dielectrics.

9. The semiconductor device of claim 8 wherein the substrate is silicon on insulator.

10. The semiconductor device of claim 8 wherein the first material is polysilicon.

11. The semiconductor device of claim 8 wherein the second material is selected from the group consisting of a metal, a metal alloy, a metal silicide, and a combination thereof.

12. The semiconductor device of claim 8 wherein the second material includes a plurality of materials.

13. The semiconductor device of claim 8 wherein at least one gate dielectric is an oxide.

14. The semiconductor device of claim 8 wherein at least one gate dielectric is a high K material.

15. A semiconductor device comprising:

a substrate;

a plurality of first gate electrodes located on the substrate;

a first gate dielectric located between each first gate electrode and the substrate, the first gate dielectrics being substantially the same thickness;

at least one of the first gate electrodes made of a first material;

at least one of the first gate electrodes made of a second material which is different from the first material;

at least one second gate electrode located on the substrate, the at least one second gate electrode being made of a third material which is different from the first and second material; and

a second gate dielectric located between each at least one second gate electrode and the substrate, the second gate dielectrics having a thickness different from that of the first gate dielectrics.

16. The semiconductor device of claim 15 wherein the substrate is silicon on insulator.

17. The semiconductor device of claim 15 wherein the first material is polysilicon.

18. The semiconductor device of claim 15 wherein the second material is a metal or metal alloy.

19. The semiconductor device of claim 15 wherein the third material is a metal silicide.

20. The semiconductor device of claim 15 further wherein the third material is a plurality of materials.

21. The semiconductor device of claim 15 wherein at least one gate dielectric is an oxide.

22. The semiconductor device of claim 15 wherein at least one gate dielectric is a high K material.

23. A semiconductor device comprising:

a substrate;

a metal gate electrode located on the substrate; and

a plurality of spacers, the plurality of spacers including a first spacer adjacent to the metal gate electrode and a second spacer adjacent to the first spacer.

24. The semiconductor device of claim 23 wherein the metal gate electrode is a metal silicide.

25. The semiconductor device of claim 23 wherein the first spacer or second spacer is selected from the group consisting of SiON, Si_3N_4, SiC, and a combination thereof.

26. A semiconductor device comprising:

a substrate;

a gate electrode located on the substrate;

a first spacer surrounding the gate electrode and spaced apart from the gate electrode to form a first region therebetween; and

a second spacer located both inside and outside of the first region.

27. The semiconductor device of claim 26 wherein the gate electrode is a metal silicide.

28. The semiconductor device of claim 26 wherein the first spacer or second spacer is selected from the group consisting of SiON, Si_3N_4, SiC, and a combination thereof.

29. A semiconductor device comprising:

a substrate;

a gate electrode located on the substrate;

a first spacer located on the substrate and adjacent to the gate electrode;

a second spacer located adjacent the first spacer, which surrounds the gate electrode and is spaced apart from the gate electrode to form a first region therebetween; and

a third spacer located both inside and outside of the first region.

30. The semiconductor device of claim 29 wherein the gate electrode is a metal silicide.

31. The semiconductor device of claim 29 wherein the first spacer is SiO_2.

32. The semiconductor device of claim 29 wherein the second spacer or third spacer is selected from the group consisting of SiON, Si_3N_4, SiC, and a combination thereof.

33. A method for manufacturing a metal gate on a semiconductor device comprising:

providing a substrate including a gate electrode located on the substrate;

forming a plurality of layers, including a first layer located on the substrate and the gate electrode and a second layer adjacent the first layer;

etching the layers to form a plurality of adjacent spacers, including a first spacer located on the substrate and adjacent the gate electrode and a second spacer adjacent the first spacer;

etching the first spacer;

forming a metal layer on the device immediately adjacent to the gate electrode; and

reacting the metal layer with the gate electrode.

34. The method of claim 33 wherein the gate electrode is polysilicon.

35. The method of claim 33 wherein the first layer and first spacer are SiO_2.

36. The method of claim 33 wherein the second layer and the second spacer are Si_3N_4.

37. The method of claim 33 wherein the plurality of layers are formed by chemical vapor deposition.

38. The method of claim 33 wherein the first spacer is etched so that its top surface is substantially the same height as the bottom surface of the second spacer.

39. The method of claim 33 wherein metal layer is Ni.

40. The method of claim 33 wherein reacting the metal layer with the gate electrode results in a NiSi gate electrode.

41. The method of claim 33 further comprising:
etching the layers to expose the substrate; and
doping the substrate to form a source and a drain.

42. The method of claim 41 further comprising:
reacting the metal layer with the substrate to form contacts for the source and the drain.

43. The method of claim 33 further comprising:
etching the unreacted metal layer;
forming a contact etch stop layer on the device.

44. The method of claim 43 wherein the contact etch stop layer is selected from the group consisting of SiON, Si_3N_4, and a combination thereof.

45. A method for manufacturing a metal gate on a semiconductor device comprising:
providing a substrate including a gate electrode located on the substrate;
forming an offset layer;
etching the offset layer to form an offset spacer adjacent to the gate electrode;
forming a plurality of layers, including a first layer located on the substrate and the gate electrode and a second layer adjacent the first layer;
etching the layers to form a plurality of adjacent spacers, including a first spacer located on the substrate and adjacent the gate electrode and a second spacer adjacent the first spacer;
etching the first spacer;
forming a metal layer on the device that is immediately adjacent to the gate electrode; and
reacting the metal layer with the gate electrode.

46. The method of claim 45 wherein the gate electrode is polysilicon.

47. The method of claim 45 wherein the first layer and first spacer are SiO_2.

48. The method of claim 45 wherein the second layer and the second spacer are Si_3N_4.

49. The method of claim 45 wherein the plurality of layers and the offset layer are formed by chemical vapor deposition.

50. The method of claim 45 wherein the first spacer is etched so that its top surface is substantially the same height as the bottom surface of the second spacer.

51. The method of claim 45 wherein metal layer is Ni.

52. The method of claim 45 wherein reacting the metal layer with the gate electrode results in a NiSi gate electrode.

53. The method of claim 45 further comprising:
etching the layers to expose the substrate; and
doping the substrate to form a source and a drain.

54. The method of claim 53 further comprising:
reacting the metal layer with the substrate to form contacts for the source and the drain.

55. The method of claim 45 further comprising:
etching the unreacted metal layer;
forming a contact etch stop layer on the device.

56. The method of claim 55 wherein the contact etch stop layer is selected from the group consisting of SiON, Si_3N_4, and a combination thereof.